TRI-GATE LOW POWER DEVICE
AND METHOD FOR MANUFACTURING THE SAME

ABSTRACT OF THE DISCLOSURE

The present invention provides a tri-gate lower power device and method for fabricating that tri-gate semiconductor device. The tri-gate device includes a first gate [455] located over a high voltage gate dielectric [465] within a high voltage region [460], a second gate [435] located over a low voltage gate dielectric [445] within a low voltage core region [440] and a third gate [475] located over an intermediate core oxide [485] within an intermediate core region [480]. One method of fabrication includes forming a high voltage gate dielectric layer [465] over a semiconductor substrate [415], implanting a low dose of nitrogen [415a] into the semiconductor substrate [415] in a low voltage core region [440], and forming a core gate dielectric layer [445] over the low voltage core region [440], including forming an intermediate core gate dielectric layer [485] over an intermediate core region [480].